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**Complete if Known**

Application Number	10/773,900
Filing Date	02/06/2004
First Named Inventor	Samir Chaudhry
Art Unit	2811
Examiner Name	Unassigned
Attorney Docket Number	Chaudhry 28-20-10-14-4/075903-289

Sheet	1	of	2
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## U. S. PATENT DOCUMENTS

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## FOREIGN PATENT DOCUMENTS

PHAT X. CAD

10/18/05

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Substitute for form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		<b>Complete If Known</b>			
		Application Number	10/773,900		
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Sheet	2	of	2	Attorney Docket Number	Chaudhry 28-20-10-14-4/075903-289

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
R	1	DUDEK, ET AL, "Lithography-Independent Nanometer Silicon MOSFET's on Insulator", IEEE Transactions on Electron Devices, Vol. 43, No. 10, October 1996, pp. 1626-1631.	
R	2	RISCH, ET AL, "Vertical MOS Transistors with 70 nm Channel Length", IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1495-1498.	
R	3	TAKATO, ET AL, "Impact of Surrounding Gate Transistor (SGT) for Ultra-High-Density LSI's", IEEE Transactions on Electron Devices, Vol. 38, No. 3, March 1991, pp. 573-577.	
R	4	TAKATO, ET AL, "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSIs", IEDM 1988, pp. 222-225.	
R	5	HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFET: A 50-nm Vertical MOSFET with Lithography-Independent Gate Length", Technical Digest of IEDM, 1999, pp. 75-78.	
R	6	OH, ET AL, "50 nm Vertical Replacement-Gate (VRG) pMOSFETs", IEEE 2000.	
R	7	HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFET: A High Performance Vertical MOSFET with Lithography-Independent Critical Dimensions", no publication information apparent from document.	
R	8	MONROE, ET AL, "The Vertical Replacement-Gate (VRG) Process for Scalable, General-purpose Complementary Logic", Paper 7.5, pp. 1-7, date and publication information unknown.	

Examiner Signature	PHAT X. CAO	Date Considered	10/18/05
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